## General Description

The MAX17242 evaluation kit (EV kit) demonstrates the MAX17242 high-voltage, current-mode step-down converters with low operating current. The EV kit operates over a wide 3.5 V to 36 V input range and the output is set for 3.3 V at 2 A .
The EV kit comes with the MAX17242ETPB installed.

## Features

- Wide 3.5 V to 36 V Input Supply Range
- 96\% Peak Efficiency @ 3.5V Input in Skip Mode
- Forced-PWM or Skip-Mode Operation
- Programmable Switching Frequency (400kHz Default)
- Selectable Spread Spectrum Optimizes EMI Performance
- FSYNC Input and Power-Good Output
- Proven 4-Layer 2oz Copper PCB Layout
- Demonstrates 950 mil x 835 mil Solution Size
- Fully Assembled and Tested


## Quick Start

## Required Equipment

- MAX17242EV kit
- 12V, 2A DC power supply
- Electronic load capable of 2A
- Digital voltmeter (DVM)


## Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation. Caution: Do not turn on supplies until all connections are made.

1) Verify that jumpers JU1-JU4 are in their default positions, as shown in Table 1 through Table 4.
2) Connect the power supply between the VINSUPSW and nearest PGND 2-hole pads or test points.
3) Connect the 2A electronic load between the VOUT and nearest PGND 2-hole pads or test points.
4) Connect the DVM between the VOUT and nearest PGND test points.
5) Turn on the power supply.
6) Enable the electronic load.
7) Verify that the voltage at the VOUT test point is approximately 3.3 V .

Table 1. EN Configuration (JU1)

| SHUNT <br> POSITION | EN PIN | MODE |
| :---: | :---: | :---: |
| $1-2^{*}$ | Connected to SUP | Normal Operation |
| $2-3$ | Connected to PGND | Shutdown Mode |

*Default position.
Table 2. Operating-Mode and Frequency Control (JU2)

| SHUNT <br> POSITION | FSYNC PIN | MODE |
| :---: | :--- | :--- |
| $1-2^{*}$ | Connected to BIAS | Forced-PWM mode |
| $2-3$ | Connected to <br> AGND | Skip mode |
| Not installed | Connected to <br> FSYNC test point <br> and external clock | Forced-PWM mode <br> (device syncs to an <br> external clock) |

*Default position.
Table 3. Spread Spectrum (JU3)

| SHUNT <br> POSITION | SPS PIN | MODE |
| :---: | :--- | :--- |
| $1-2^{*}$ | Connected to BIAS | Spread-Spectrum <br> Enabled |
| $2-3$ | Connected to <br> AGND | Spread-Spectrum <br> Disabled |

*Default position.
Table 4. PGOOD (JU4)

| SHUNT POSITION | MODE |
| :---: | :---: |
| Installed* $^{*}$ | PGOOD pulled high to BIAS |
| Not installed | PGOOD pulled high to V_PULL |

*Default position.

Ordering Information appears at end of data sheet.

## Detailed Description of Hardware

The MAX17242EV kit demonstrates the MAX17242 highvoltage, high-frequency, step-down converter with low operating current. The EV kit operates over a wide 3.3 V to 36 V input range and the output is set for 3.3 V at 2 A . Consider thermal and switching efficiency when designing for operation in the $24 \mathrm{~V}-36 \mathrm{~V}$ input voltage range.

## Enable (EN)

Place a shunt in the 1-2 position on JU1 for normal operation. To place the device into shutdown mode, move the shunt on JU1 to the 2-3 position.

## Synchronization Input (FSYNC)

The EV kit features jumper JU2 to control the synchronization input (FSYNC). The device synchronizes to an external signal applied to FSYNC. Connect FSYNC to AGND to enable skip-mode operation. Connect to BIAS to enable Forced-PWM mode, or to an external clock to enable fixed-frequency forced-PWM mode operation.
To use an external clock, uninstall the shunt on jumper JU2 and apply the signal at the FSYNC test point and AGND. The external clock frequency at FSYNC can be higher or lower than the internal clock by $20 \%$. Ensure that the duty cycle of the external clock used has a minimum 100ns pulse width. The external clock logic High voltage can be in the in the $1.4 \mathrm{~V}-5 \mathrm{~V}$ range.

## Spread-Spectrum Option (SPS)

The EV kit provides jumper JU3 that allows SPS to be pulled high (BIAS) or pulled low (AGND). Connect SPS high to enable spread spectrum where the operating frequency is varied $\pm 3 \%$ centered on FOSC. Connect SPS low to disable the spread-spectrum feature.

## Setting the Switching Frequency (FOSC)

The EV kit switches at 400 kHz by default, and the switching frequency is set by a resistor, RFOSC (R4), connected from FOSC to AGND. Refer to TOC08 in the Typical Operating Characteristics section of the MAX17242 IC data sheet for the correct RFOSC (R4) value.

## Power-Good Output (PGOOD)

The EV kit provides a PGOOD test point to monitor the status of the device output. PGOOD asserts when VOUT rises above $95 \%$ of its regulation voltage. PGOOD deasserts when $V_{\text {OUT }}$ drops below $92.5 \%$ of its regulation voltage. R5 pulls PGOOD up to BIAS or V_PULL with respect to AGND. When operating in Skip-mode, use an external voltage source for V_PULL. Remove the shunt on jumper JU4 and connect an external voltage source up to 5.5 V to the V_PULL 2-hole pad.

## Output

Resistor R6 connects FB to BIAS for a fixed +3.3 V (EV kit default output) or a fixed +5 V output voltage. To set the output to other voltages between 1 V and 10 V , connect a resistive divider from output (OUT) to FB to AGND. Use the following equation to determine the R7 and R8 of the resistive divider network:

$$
\mathrm{R} 7=\mathrm{R} 8 \times\left(\frac{\mathrm{V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{FB}}}-1\right)
$$

where $V_{F B}=1 \mathrm{~V}$ and R 8 is $\leq 500 \mathrm{k} \Omega$.

## Operation at 1 MHz Switching Frequency

For 1 MHz switching frequency, the following components must be changed to:

- $\mathrm{R} 4=27.4 \mathrm{k} \Omega$
- $\mathrm{L} 1=4.7 \mu \mathrm{H}$ (recommend Coilcraft XAL6060-472MEB)
- $\mathrm{R} 1=12.1 \mathrm{k} \Omega$
- $\mathrm{C} 10=6,800 \mathrm{pF}$

Additional capacitance on C8 may be needed, depending on transient performance.

Component Suppliers

| SUPPLIER |  |
| :--- | :--- |
| Coilcraft Inc. | www.coilcraft.com |
| Murata Americas | www.murata.com |
| Panasonic Corp. | www.panasonic.com |
| TDK Corporation | www.tdk.com |

Note: Indicate that you are using the MAX17242 when contacting these component suppliers.

## MAX17242 EV Bill of Materials

| REF_DES | QTY | DESCRIPTION |
| :---: | :---: | :--- |
| C1, C3 | 2 | CAPACITOR; SMT (0603); CERAMIC CHIP; 0.1UF; 100V; TOL=10\%; TG=-55 DEGC TO +125 DEGC; <br> TC=X7R |
| J1-J3, J5 | 4 | CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT THROUGH; 3PINS; -65 DEGC TO <br> +125 DEGC |
| J4 | 1 | CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 4PINS |
| LED1 | 1 | DIODE; LED; LY L29K SERIES; SMARTLED; YELLOW; SMT (1608); VF=1.8V; IF=0.02A |
| LED2 | 1 | DIODE; LED; SMART; RED; SMT (0603); PIV=1.8V; IF=0.02A; -40 DEGC TO +100 DEGC |
| R1 | 1 | RESISTOR; 0603; 5K OHM; 0.1\%; 25PPM; 0.15W; THIN FILM |
| SU1-SU5 | 5 | TEST POINT; JUMPER; STR; TOTAL LENGTH=0.24IN; BLACK; INSULATION=PBT;PHOSPHOR <br> BRONZE CONTACT=GOLD PLATED |
| TP1 | 1 | TESTPOINT WITH 1.80MM HOLE DIA, RED, MULTIPURPOSE; |
| TP2-TP6, | 6 | TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; WHITE; PHOS- <br> PHOR BRONZE WIRE SILVER PLATE FINISH; |
| TP8 | 6 | TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; BLACK; PHOS- <br> PHOR BRONZE WIRE SILVER PLATE FINISH; |
| TP9-TP11 | 3 | IC; DRV; 24V PIN-CONFIGURABLE INDUSTRIAL SENSOR OUTPUT DRIVERS; TDFN12-EP |
| U1 | 1 | PACKAGE OUTLINE 0603 NON-POLAR CAPACITOR |
| C4 | 0 | 1 |
| PCB | 1 | PCB Board:MAX14838 EVALUATION KIT |

## MAX17242 Evaluation Kit with Preset

## MAX17242 EV Schematics



MAX17242 EV Schematic


MAX17242 EV Minimal Component Schematic

## MAX17242 EV PCB Layout



MAX17242 EV Top Silkscreen


MAX17242 EV Bottom Silkscreen


MAX17242 EV Component Side


MAX17242 EV Solder Side

MAX17242 EV PCB Layout (Continued)


MAX17242 EV Layer 2-PGND

Ordering Information

| PART | TYPE |
| :---: | :--- |
| MAX17242EVKIT\# | EV Kit |

\#Denotes RoHS compliant.

## Revision History

| REVISION <br> NUMBER | REVISION <br> DATE | DESCRIPTION | PAGES <br> CHANGED |
| :---: | :---: | :--- | :---: |
| 0 | $12 / 15$ | Initial release | - |
| 1 | $5 / 16$ | Updated Table 2 | 1 |
| 2 | $8 / 16$ | Removed FSYNC information in Table 2 | 1 |

